

Art Unit: 2829

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SD

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CLAIM 1 IS CANCELLED

2. (Currently Amended) ~~The test circuit of claim 1~~

A test circuit comprising:

a first transistor pair including a first transistor and a second transistor coupled with a device under test; and

a second transistor pair including a third transistor and a fourth transistor coupled with a dummy device, the first transistor and the third transistor having a first common gate connection configured to be driven by a first variable voltage, the first transistor and the third transistor being biased by a first variable bias voltage, the second transistor and the fourth transistor having a second common gate connection configured to be driven by a second variable voltage, the second transistor and the fourth transistor being biased by a second variable bias voltage, wherein the first transistor and the third transistor each comprise a p-channel transistor and the second transistor and the fourth transistor each comprise a p-channel transistor.

3. (Original) The test circuit of claim 2 wherein:

the first transistor has a drain coupled to the device under test; and
the second transistor has a source coupled to the device under test.

4. (Original) The test circuit of claim 3 wherein:

the third transistor has a drain coupled to the dummy device; and
the fourth transistor has a source coupled to the dummy device.

5. (Original) The test circuit of claim 4 where the first transistor, the second transistor, the third transistor and the fourth transistor are formed in an n-well on a p-substrate.

6. (Original) The test circuit of claim 5 wherein the first transistor is substantially matched to the third transistor and the second transistor is substantially matched to the fourth transistor.

7-10. (Cancelled)

11. (Currently Amended) The test circuit of claim ~~[[1]]~~ 2 further comprising a clock signal generating circuit coupled with the first common gate connection and the second common gate connection and configured to generate the first variable voltage and the second variable voltage.

12. (Original) The test circuit of claim 11 wherein the clock signal generating circuit comprises:

an oscillator; and

a frequency division circuit for reducing frequency of signals generated by the oscillator to provide for allowing monitoring frequencies of the first variable voltage and the second variable voltage.

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13. (Original) The test circuit of claim 12 wherein the frequency division circuit comprises one or more counters.

14. (Original) The test circuit of claim 11 wherein the clock signal generating circuit comprises one or more voltage controlled oscillators.

15. (Original) The test circuit of claim 14 wherein the clock signal generating circuit further comprises circuitry to control frequency division of the signals generated by the oscillator.

16-18. (Cancelled)

19. (Currently Amended) The test circuit of claim ~~[[1]]~~ 2 wherein the device under test and the dummy device comprise multiple electrode capacitances.

CLAIMS 20 THROUGH 108 ARE CANCELLED